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Atty. Docket No. MIO 0012 V2

Rejections under 35 USC §112

Claims 31 and 32 have been rejected under 35 USC §112, first paragraph as containing subject matter which was not described in the specification. Claim 31 has been amended to recite subject matter having clear support in the specification. Basis for the amendment is provided in Figs. 4-5 and page 8, lines 8-20.

In addition, the Examiner states that the insulating layer must be formed between the semiconductor layer 22 and the conductive layer 26 to provide electrical isolation. At page 8, lines 14-18, it is taught that the insulating layer may not be necessary. Thus, claim 31 is in compliance with 35 USC §112, first paragraph. Claim 32 has been rejected as depending from a rejected base claim. Since claim 31 is in compliance with 35 USC §112, first paragraph, claim 32 is now in compliance with 35 USC §112, first paragraph.

Rejections under USC § 102 (e)

Claims 21-24 and 31-32 have been rejected under 35 USC §102 (e) as being anticipated by Zamanian (U.S. Patent No. 5,793,111). Zamanian teaches a semiconductor integrated circuit having an improved landing pad. Referring to Fig. 6, Zamanian teaches an oxide layer 28 that includes an opening 30 formed through the oxide layer 28. A polysilicon layer 32 is formed over the oxide layer 28 and the contact opening 30. A silicide layer 36 is formed over the polysilicon layer 32. A barrier layer 34 is formed over the silicide layer 36. A dielectric layer 40, contact opening 42, and conductive contact 44 are formed, wherein barrier layer 34 is located in the bottom of the contact opening underlying the aluminum layer 44. See col. 5 lines 49-63.

The Examiner states that the silicide layer 36, shown in Fig. 5, or the barrier layer 34, shown in Fig. 6, allow the conductive contact 44 to electrically contact the vertical component of conductive material 32. The Examiner further states that the method as claimed does not preclude including an additional conductive layer therebetween. Claim 21, as amended, recites "forming a contact in said overlayer and in said vertical component disposed adjacent to and directly contacting said vertical component." Zamanian does not teach that the contact is formed in the contact hole directly contacting

the vertical component. Rather, Zamanian only teaches the bottom of the conductive contact 44 being either the silicide layer 36 or the barrier layer 34. See Fig. 5; Fig. 6; and col. 5, lines 61-63. The silicide layer 36, as shown in Fig. 5, or the barrier layer 34, as shown in Fig. 6, do not allow the conductive contact 44 to directly contact the vertical component of conductive material 32 formed in the oxide layer 28. Thus, every element of claim 21, as amended, is not taught. Claims 22-24 depend from claim 21, therefore, applicants respectfully request that this rejection to claims 21-24 be withdrawn. Furthermore, Zamanian does not even suggest forming the contact in the overlayer directly contacting the vertical component and then filling that contact with a conducting material.

Claim 31, as amended, to recites "forming a contact in said overlayer and in said vertical component disposed adjacent to and contacting said vertical component." As explained above, Zamanian does not teach that the contact is in direct contact with the vertical component. The contact cannot be in the vertical component if the contact does not even directly contact the vertical component. Therefore, every element of claim 31, as amended, is not taught. Claim 32 depends from claim 31, thus, applicants respectfully request that this rejection to claims 31 and 32 be withdrawn. Furthermore, Zamanian does not even suggest having a contact in the overlayer and in the vertical component.

Claims 31-32 have been rejected under 35 USC § 102 (e) as being anticipated by Okada (U.S. Patent No. 5,399,890). Okada et al. teach a semiconductor memory that includes an isolation region 2 and transistors 3a and 3b formed on a semiconductor substrate 1. A bit line 4 of a metal or silicide or polycide is formed on the semiconductor substrate on which a first interlayer insulating film 5 is deposited. Contact holes 6 and 6a are formed after which a conductive layer is formed. The conductive layer is patterned to form node electrode 7a and a first level interconnection layer 7b. A capacitance insulating film 8 is then formed over the node electrode 7a and the first level interconnection layer 7b. The capacitance insulating film 8 is etched to form a plate electrode 9. A second interlayer insulating film 10, formed of silicon oxide, is formed over the plate electrode 9. Contact holes 11 that reach designated regions of the plate

electrode 9 and the first level interconnection layer 7b are opened through the second interlayer insulating film 10.

Applicants respectfully traverse the rejection as every element of the claimed invention is not taught by Okada et al. Okada et al. do not teach "forming a contact in said overlayer and in said vertical component disposed adjacent to and contacting said vertical component." Rather, Okada et al. teach a contact 11 that is formed in the overlayer 10. However, the contact 11 does not extend to the vertical component of the conductive layer. The contact 11 in Figs. 2C and 3 may touch the conductive layer 9, but the contact does not extend into the vertical component of layer 9. Every element of claim 31 is not taught, therefore, claim 31 is novel over Okada. Claim 32 depends from claim 31, therefore, claim 32 is novel over Okada. Furthermore, Okada does not even suggest having the contact 11 in the vertical component of conductive layer 9.

Rejections under §103 (a)

Claims 21-25 and 31-32 have been rejected under 35 USC § 103 (a) as being unpatentable over Matsuo et al. (U.S. Patent No. 5,312,769) taken with Zamanian and Wolf (pages 547-554). Matsuo et al. teaches a p-type silicon substrate having a n+-type diffused region formed in the silicon substrate 1, a gate oxide film 4 formed on the silicon substrate, an insulting film 21, and a first interlayer insulating film 23 formed on the insulating film 21 covering first and second polycrystalline silicon lead pads 12 and 22. The first interlayer insulating film 23 is not overetched when forming the contact hole. Zamanian is explained above. Wolf teaches a basic etching of silicon and silicon dioxide with fluorocarbon-containing plasma along with anisotropy etching. Wolf indicates that while etching SiO_2 the underlying Si layer may be etched, but not significantly. See page 549.

In the amendment faxed on October 24, 2002, applicants argued that Zamanian and Wolf teach away from one another as Wolf teaches only incidental overetching with Zamanian teaching significant overetching. The Examiner argues that both Wolf and Zamanian teach the necessity to overetch and therefore do not teach away from one

another. Applicants respectfully disagree and believe that applicants' previous argument may have been misinterpreted by the Examiner.

Wolf does not teach that overetching is a "necessity," rather Wolf teaches away from overetching. Wolf explains that the etching rates of Si and SiO_2 are different under the same conditions. Thus, SiO_2 can be etched when Si will not be etched, and if overetching does occur, the overetching is not significant. See page 549. However, there is no teaching that overetching is necessary. More specifically, Fig. 9 of Wolf shows that the etch rate of Si decreases as the percentage of H_2 increases. The etch rate of SiO_2 remains almost constant as the percentage of H_2 increases. This allows the SiO_2 layer to continue to be etched under conditions when etching of the Si has ceased. See page 550. Thus, the SiO_2 can be selectively etched over Si. See page 550.

Zamanian teaches overetching a barrier layer to insure that all of the dielectric layer 40 has been removed from the contact opening. See col. 6, lines 1-4. Thus, Wolf is not combinable with Zamanian as Wolf teaches away from significantly overetching.

The Examiner next states that even if it is not obvious to combine Wolf with Zamanian, it still would have been obvious to form the contact hole of Okada et al by etching a contact hole in the overlayer insulator and in an overetch amount of the layer of conductive material having a substantially vertical component, as combinatively taught by Zamanian and Toshiyuki. The rejection did not mention or rely upon Okada or Toshiyuki previously. Applicants believe that rather than Okada and Toshiyuki, the Examiner meant Matsuo and Wolf, respectively. Therefore, applicants will argue in this manner.

Applicants reiterate their argument from the amendment faxed on October 24, 2002. The combination of Matsuo et al. with Zamanian and Wolf does not teach the claimed invention. The result of the combined teachings as suggested by the Examiner would be the contact hole of Mastuo et al. extending through the barrier layer of Zamanian possibly barely scratching the surface of the silicide layer, as taught by Wolf.

Another possible result would be the contact hole of Mastuo et al. extending through the barrier layer and the silicide layer of Zamanian and, as taught by Wolf, possibly barely scratching the surface of the polysilicon layer of Zamanian. Neither result teaches or suggests the claimed invention. Specifically, the claimed invention teaches forming a contact in the contact hole that is **directly contacting** the vertical component, simply scratching the surface of the polysilicon layer would not contact the vertical component. Thus, claim 21 is patentable over Mastuo et al. taken with Zamanian and Wolf. Claims 22-25 depend from claim 21, therefore, claims 22-25 are also nonobvious over Mastuo et al. taken with Zamanian and Wolf.

Claim 31, as amended, recites "forming a contact in said overlayer and in said vertical component disposed adjacent to and contacting said vertical component." Applicants rely on the arguments above. Simply scratching the surface of the polysilicon layer would not cause the layer to be **in** the vertical component. Thus, claim 31 is not obvious over Mastuo et al. taken with Zamanian and Wolf. Claim 32 depends from claim 21, therefore, claim 32 is also nonobvious over Mastuo et al. taken with Zamanian and Wolf.

Claims 21-25 and 31-32 have been rejected under 35 USC § 103 (a) as being unpatentable over Okada et al. taken with Zamanian and Toshiyuki et al. (JP-05-109905). Toshiyuki et al. teach etching of an insulating layer 3 to form an opening in the contact layer 2 and filling this contact layer 2 with an electrode layer 6. Claim 21 has been amended to recite "forming an underlayer having an opening over the at least one semiconductor layer; forming a layer of conductive material over the underlayer and said opening having a topography that includes a substantially vertical component."

The Examiner states that Toshiyuki teaches forming a conductive material 2 over an underlayer in Fig. 2, then forming an overlayer 3 over the layer of conductive material. The conductive material 2 does not contain a substantially vertical component as recited in claim 21 as amended. Rather, Toshiyuki teaches a first wiring layer that is formed over a semiconductor substrate. There is no underlayer having an opening and

conductive material that has a substantially vertical component as claimed. Toshiyuki teaches that the first wiring layer will not have a substantially vertical component as the base is almost flat. See paragraph 0015. Only the second wiring layer has a substantially vertical component. However, this substantially vertical component is formed by etching the overlayer in an overetched amount, then forming the second wiring layer over the overlayer. Okada and Zamanian teach a vertical component that is formed in an underlayer rather than in the overlayer. Thus, one of ordinary skill in the art would not combine Toshiyuki et al. with Zamanian or Okada et al. because Toshiyuki et al. teaches away from the methods taught by Zamanian and Okada et al.

Even if the reference teachings were combined, the present invention would not result. A combination of the references in the manner suggested by the Examiner would result in the contact hole of Okada et al. being formed in an overetched portion of the landing pad, the landing pad having a flat base over the substrate (as taught in Toshiyuki et al.), wherein the overetched portion is the barrier layer of Zamanian. This is not the invention recited in claim 21, as amended. Thus, claim 21 is nonobvious over Okada in view of Zamanian and Toshiyuki. Claims 22-25 depend from claim 21, therefore, claims 22-25 are nonobvious over the combination.

Claim 31, as amended, recites "forming a structure having an opening in said at least one semiconductor layer; forming a layer of conductive material over said at least one semiconductor layer; filling said opening with said conductive material to form a substantially vertical component; forming an overlayer over said layer of conductive material." As stated above, these limitations are not taught or suggested by Okada in view of Zamanian and Toshiyuki. Thus, claim 31 is nonobvious over the combination. Claim 32 depends from claim 31, thus, claim 32 is also nonobvious.

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In CONCLUSION

Applicants respectfully submit that, in view of the above remarks, the application is now in condition for allowance. Early notification of allowable subject matter is respectfully solicited.

Respectfully submitted,

KILLWORTH, GOTTMAN, HAGAN & SCHAEFF, L.L.P.

By Julie Cope

Julie G. Cope
Registration No. 48,624

One Dayton Centre
One South Main Street, Suite 500
Dayton, Ohio 45402-2023
Telephone: (937) 223-2050
Facsimile: (937) 223-0724

JGC/